NASA Electronic Parts and Packaging Program (NEPP)

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FY01 Proposal

Title: Enhanced Reliability of Microelectronic Circuits Interconnects Using Microwave Radiation

(check one): New Proposal

Total $ Requested for FY01: $ 140,000

Technology Type: Advanced/Emerging

Project Area: Packaging

Proposing Centers: JPL

Participating Center(s): ☐ % GSFC ☐ % G ☐ % LaR ☐ 100% JPL ☐ % MSFC ☐ % JSC ☐ Other

(Estimated Center Participation, %$): JPL 100%, $140K

Collaborators: Electronic Packaging and Fabrication Section (JPL Section 349)

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OBJECTIVE (S):

- Validate a repair process for microcircuit interconnect defects, such as small signal lines, microvias, and damaged gate metallization. Other intricate repairs such as local reflow of solder balls in ballgrid and flip chip arrays will be evaluated and validated.
- Demonstrate enhanced reliability of microelectronic circuits and document the increase in operational lifetimes of these devices.

Task Description:

We expect to evaluate the feasibility of microcircuit repair and improved circuit reliability in a two-phase effort. The first phase will validate this local repair technique utilizing test coupons of representative structures. The second phase will utilize actual functional circuits incorporating live die and other active devices.

All validation work will be performed at JPL, but some of the NDE testing may utilize equipment at other NASA centers.

Task Approach To Meeting NEPP Objectives:

- The results of this task will produce concrete **processes for reliability enhancement** in microelectronic devices and **data for reliability assessment** of the devices processed.
- The results of this task will include **recommendations to improve** the present state of the art reliability processes based on our microwave annealing technique.
- All of this work including test reports and publications will be made available and distributed to the NASA and industrial community electronically and through print.

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Technical Background: The issue of electronic-circuit reliability is becoming increasingly important to applications in space exploration and to the military. Failure in electronic circuits, in many cases, is due to the creation of defects (voids in the interconnect) by the stresses applied to the interconnects. These stresses are caused by mismatches in thermal expansion coefficients between the substrate and the interconnects. The constant demand for device miniaturization increases the stress on interconnects. The higher aspect ratio of these interconnects exacerbates the problem of stress-induced failures. Relieving the stress in these circuit interconnects, to solve this problem, is not possible with conventional thermal cycling. However, by using microwave techniques one has the ability to "selectively heat" the interconnects only. We have used and documented the ability of microwave radiation to selectively heat copper interconnects in earlier studies[1]. The copper metallization in our study diffused in the silicon wafer tracks filling them up completely. By concentrating the power in a microwave resonant cavity, we were able to accomplish the diffusion of the copper metallization using as little power as 1 watt! In our work referenced above, we have clearly demonstrated the feasibility of using microwaves for diffusing copper metallization into silicon wafer tracks, now comes the application of this idea to the specific problem of microcircuit-interconnect defect removal. Presently, the state of the art attempts to solve this type problem by judicious placement of the interconnect within the substrate using computer modeling. This placement is claimed to minimize the effects of stress and wire cross talking.

Technical Approach:

The mismatches in the coefficients of thermal expansion for the substrates and the interconnect metallization produce large stresses on the latter. We plan to anneal this stress by selectively heating the interconnect. This is not possible by conventional heating means where the heat is conducted from outside to the inside. However, the use of microwaves allows the metallization to heat first, any heating of the substrate occurs as a consequence of this process. Therefore, the heating of the substrate is minimal. This work will be conducted inside of single-mode microwave cavity. Such a cavity hosts standing waves where power concentration is very high. This concentration allows us to use very low power (~1 watt) to be applied to the electronic circuitry to initiate the stress annealing. These experiments would be divided in a two-phase effort. In the first phase of this study, we will focus on test structures while in the second phase we will work on real devices. The overall strategy in the two phases will simply be to examine, document, and validate using standard microscopy techniques (TEM, SEM),and acoustic microscopy (C-SAM) techniques of microelectronic circuits before and after microwave heat treatment.

The results of this work are important to the overall reliability of microelectronic circuits and applicable regardless of the interconnect metallization used. It will allow device users a prolonged lifetime of their devices based on the reduction of defects in microcircuit interconnects.

This proposal would contribute to the benefit of most NASA Enterprises due to its wide range applicability. Other additional beneficiaries may include the DOD where high reliability electronics is also needed.

PHASE I

The results of this study will determine the stress annealing parameters and their optimal values. We will assess scientifically this novel technique of stress annealing microcircuits, and provide a recommendation on its utility for real devices.

PHASE II:

We will be implementing the results of previous work to real devices. We will measure the enhancement of the micro-circuitry reliability by way of determining the amount of defects eliminated by this stress annealing process. Based on this, a calculation of the anticipated life time enhancement will be obtained.

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[1] R.A. Brain, H.A. Atwater, and M. Barmatz "Rapid Selective Annealing of Cu Thin Films on Si Using Microwaves" Mat. Res. Soc. Symp. Proc. Vol. 347. (519-524) 1994 Materials research Society

The Microwave Materials Processing Lab (section 354) has acquired a great deal of expertise in this field with numerous publications in conferences and refereed journals. We have accumulated over 15 years of experience in this field.

NASA Customers: **X-2000**
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NEW MILLENIUM SERIES

Clearly Stated Deliverables:

- Reports which document and validate the annealing processes and the parameters that would minimize such failure mechanisms.
- Document all experimental results and data.
- Generate a final report on the reliability enhancement by this method and relevant recommendation for its applicability to high reliability systems.
- Publications and presentations at the appropriate forums.

Top Level Schedule:
SCHEDULE & MILESTONES:

1Q01	Experimental set up
2Q01	Test structures stress annealing study begins
3Q01	Report on all relevant parameters found plus value optimization
4Q01	Final Report on results for test structures in Phase I
1Q02	Set up modifications for real devices
2Q02	Real devices stress annealing study begins
3Q02	Report on all relevant parameters found relevant for Phase II
4Q02	Final report to assess this technique for circuit reliability improv